WHAT IS CLAIMED IS:

1. A method for testing a physical layer device including a link layer interface, a physical layer logic circuit to be connected to said link layer interface, and a plurality of ports to be connected to said physical layer logic circuit, said method characterized in that:

a test link layer circuit to be interrelated to said link layer interface and a test physical layer logic circuit to be interrelated to said physical layer logic circuit are provided beforehand in said physical layer device;

in testing, said test link layer circuit is connected to said physical layer logic circuit through said link layer interface, and said test physical layer logic circuit is connected to said physical layer logic circuit through said plurality of ports; and

said link layer interface, said physical layer logic circuit, and said plurality of ports are tested.

2. A physical layer device with test circuits, said physical layer device including a link layer interface, a physical layer logic circuit to be connected to said link layer interface, and a plurality of ports to be connected to said physical layer logic circuit, said physical layer device characterized by comprising:

a test link layer circuit for establishing, in testing, a connection with said physical layer logic circuit through said link layer interface

and communicating predetermined data with said physical layer logic circuit; and

a test physical layer logic circuit for establishing, in testing, a connection with said physical layer logic circuit through said plurality of ports and communicating predetermined data with said physical layer logic circuit.

3. A physical layer device with test circuits according to Claim 2, characterized in that:

said link layer interface includes a switch for selectively establishing a connection with an external link layer device or said test link layer circuit; and

a predetermined port from among said plurality of ports includes a switch for selectively establishing a connection with said physical layer logic circuit or said test physical layer logic circuit.

4. A transmitting/receiving circuit with test circuits, said transmitting/receiving circuit including at least a set of a driver and a receiver, characterized by comprising:

test data storage means for storing test data transmitted by said driver; and

comparison means for comparing, when said receiver receives the test data transmitted from said driver, the received test data with the test data stored in said test data storage means.

5. A transmitting/receiving circuit with test circuits according to Claim 4, characterized in that:

reception storage means for storing the received test data is provided; and

said comparison means compares the received test data stored in said reception storage means with the test data stored in said test data storage means.

6. A transmitting/receiving circuit with test circuits according to Claim 5, characterized in that:

said test data storage means and said reception storage means are formed of registers; and

the registers operate in synchronization based on the same clock.

7. A transmitting/receiving circuit with test circuits, said transmitting/receiving circuit including at least a set of a first driver and a first receiver and another set of a second driver and a second receiver, characterized by comprising:

test data storage means for storing test data transmitted by said first driver; and

comparison means for comparing, when said first receiver and said second receiver each receive the test data transmitted by said first driver, each of the received test data with the test data stored in said

test data storage means.

8. A transmitting/receiving circuit with test circuits according to Claim 7, characterized in that:

first reception storage means for storing the received test data received by said first receiver and second reception storage means for storing the received test data received by the second receiver are provided; and

said comparison means includes first comparison means for comparing the received test data stored in said first reception storage means with the test data stored in said test data storage means; and second comparison means for comparing the received test data stored in said second reception storage means with the test data stored in said test data storage means.

9. A transmitting/receiving circuit with test circuits according to Claim 8, characterized in that said test data storage means, said first reception storage means, and said second reception storage means are formed of registers; and said registers operate in synchronization based on the same clock.

10. A transmitting/receiving circuit with test circuits, said transmitting/receiving circuit including a set of a first driver and a first receiver and another set of a second driver and a second receiver, characterized by comprising:

test data storage means for storing test data;

selection means for selecting inputting of the test data to said first driver or said second driver; and

comparison means for comparing, when said first receiver and said second receiver each receive the test data transmitted by said first driver, each of the received test data with the test data stored in said test data storage means and for comparing, when said second receiver receives the test data transmitted by said second driver, the received test data with the test data stored in said test data storage means.

11. A transmitting/receiving circuit with test circuits according to Claim 10, characterized in that:

first reception storage means for storing the received test data received by said first receiver and second reception storage means for storing the received test data received by said second receiver are provided; and

said comparison means includes first comparison means for comparing the received test data stored in said first reception storage means with the test data stored in said test data storage means; and second comparison means for comparing the received test data stored in said second reception storage means with the test data stored in said test data storage means.

12. A transmitting/receiving circuit with test circuits according to Claim 11, characterized in that said test data storage means, said first

reception storage means, and said second reception storage means are formed of registers; and the registers operate in synchronization based on the same clock.

13. A transmitting/receiving circuit with test circuits according to any one of Claims 4 to 12, characterized in that said transmitting/receiving circuit is a physical layer device of an IEEE 1394 interface.